



## **Pletronics, Inc.**

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**Effective January 1, 2008**

**The LV11xxBY and the LV11xxBW devices are discontinued.**

These were discontinued because the components needed to make these parts are no longer available.

### **For the LV11xxBY**

Use the LV99xxDV oscillator and a 3.3V LDO. The board space required will be similar.

### **For the LV11xxBW**

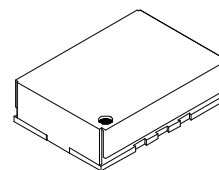
Use the LV77xxDW oscillator, this is a smaller footprint and superior performance



# Pletronics, Inc.

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Manufacturer of High Quality Frequency Control Products

## LV1145B LVDS Series



- Low Voltage Differential Signal Output with Enable/Disable
- 6 Pad Leadless Surface Mount Oscillator

**1.50 MHz – 650.00 MHz**

Consult factory for higher frequencies

### Standard Specifications

Overall Frequency Stability	± 50 PPM, ± 25 PPM and ± 20 PPM over Operating Temp. Range
Operating Temperature Range	0 to +80°C is standard, can be extended to - 40 to +85°C
Operable Supply Voltage (Vcc)	3.3 V ± 5% standard, 5.0 V ± 10% also available
High Level Output Voltage	1.43 V typical and 1.60 V maximum with output enabled (100 ohm load) See Test circuit #6
Low Level Output Voltage	0.90 V minimum and 1.10 V typical with output enabled (100 ohm load) See TC #6
Differential Output Voltage	247 V minimum, 330 V typical and 454 V maximum with output enabled (100 ohm load) See TC #6
Offset Voltage	1.125 V minimum, 1.25 V typical and 1.375 V maximum with output enabled (100 ohm load) See TC #6
Output Leakage Current	10 uA maximum with output disabled
Supply Current (Icc) Enabled	50 mA max < 200 MHz, 60 mA max < 500 MHz, 70 mA max 500 MHz and above
Supply Current (Icc) Disabled	20 mA max < 200 MHz, 30 mA max < 500 MHz, 40 mA max 500 MHz and above
Symmetry (DC)	45/55% measured at 0°C ≤ Ta ≤ 70°C, 40/60% measured at Ta < 0°C and Ta > 70°C
Rise and Fall Time (Tr & Tf)	1.0 nS max at 20% to 80% output swing (100 ohm load) See Test circuit #6 and Waveform #2
RMS Jitter	1.0 pS max at 12 kHz to 20 MHz from the output

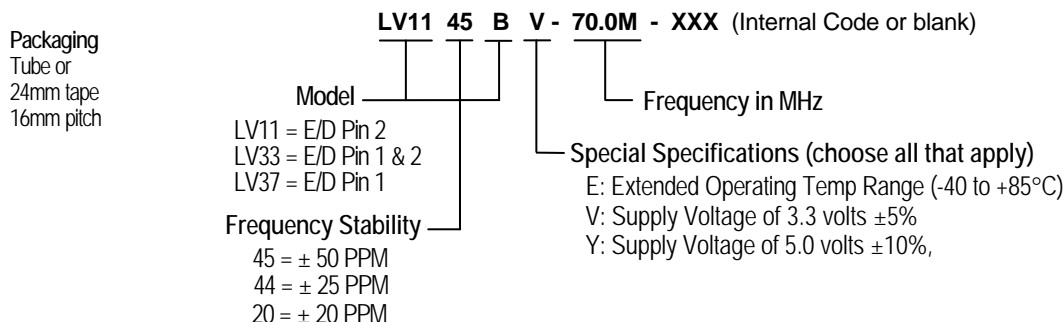
### Enable / Disable Pin:

The Enable / Disable pin has an internal pull up and if the pin is not connected the oscillator is enabled. Pletronics strongly recommends connecting the Enable / Disable pin to Vcc, if the oscillator is to be enabled at all times. In the disable condition, the output becomes a high impedance.

High Level Input Voltage	0.7 Vcc minimum at Enable / Disable Pin
Low Level Input Voltage	0.3 Vcc maximum at Enable / Disable Pin
High Level Input Current	-20 uA maximum at Enable / Disable Pin = 0.7 Vcc
Low Level Input Current	-200 uA maximum at Enable / Disable Pin = 0 V
Output Enable Time	200 nS maximum
Output Disable Time	200 nS maximum

### Part Numbering Guide

Portions of the part number that appear after the frequency may not be marked on part (C of C provided)



Consult factory for available frequencies and specs. Not all options available for all frequencies. A special part number may be assigned. Frequency Stability is inclusive of frequency shifts due to calibration, temperature, supply voltage, shock, vibration and load

Jun 2004



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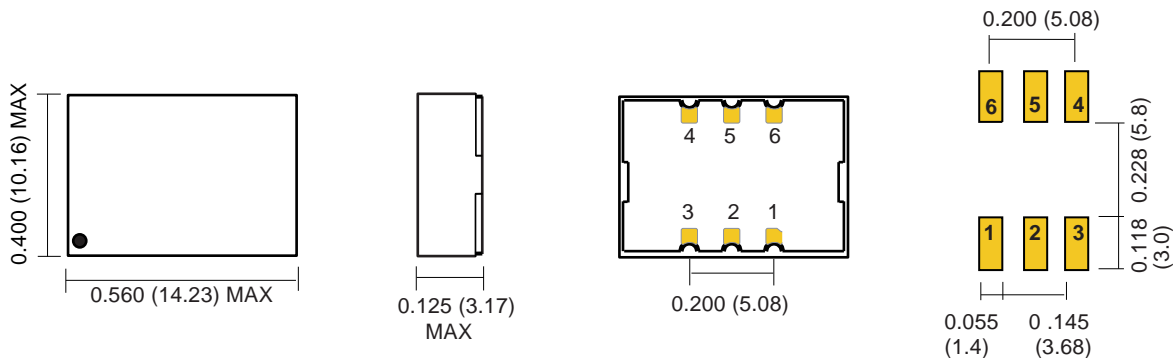
## LV1145B LVDS Series

**Mechanical: inches (mm)**

**not to scale**

**Solder Pads**

Due to part size and factory abilities, part marking may vary from lot to lot and may contain our part number or an internal code.



LV1145B

PIN	SIGNAL
1	N.C.
2	E/D
3	GND
4	VoD+
5	VoD-
6	Vcc

1.50 - 650.0 MHz

LV3345B

PIN	SIGNAL
1	E/D
2	E/D
3	GND
4	VoD+
5	VoD-
6	Vcc

120.0 - 650.0 MHz (5.0 Vcc - May not be available)  
 180.0 - 650.0 MHz (3.3 Vcc)

LV3745B

PIN	SIGNAL
1	E/D
2	N.C.
3	GND
4	VoD+
5	VoD-
6	Vcc

See page 6 for Layout Guidelines



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## PECL and LVDS Layout Guidelines

**SUGGESTED PCB LAYOUTS**

Solder Pad Layout which accommodates all PECL surface mount devices

0.200 (5.08)  
 0.185 (4.7)  
 0.087 (2.2)  
 0.055 (1.4) 0.100 (2.54)

'B Pkg'  
 5 x 7

TOP SIDE BYPASS

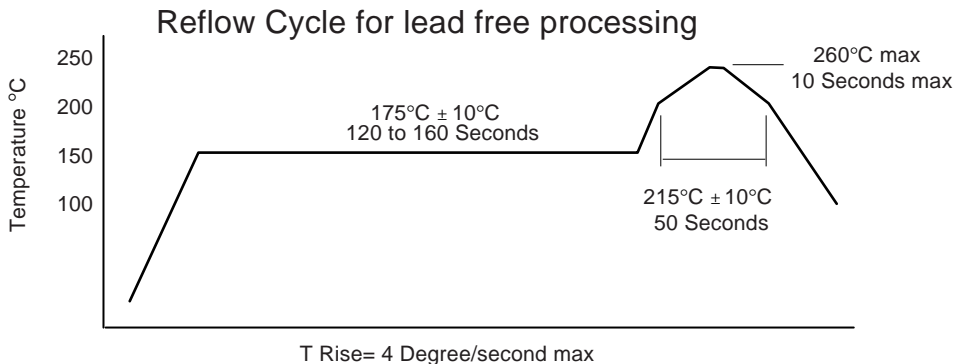
BOTTOM SIDE BYPASS

MULTI LAYER BYPASS

The output line should be designed with proper characteristic impedance. Pletronics recommends laying out for the larger 'B package' with pads long enough to accept the smaller 5 x 7mm device. This permits the best option for alternate sources of device. Pletronics also recommends connecting Pin 1 and Pin 2 together on the models with Q & QN OUT on pins 4 & 5. This allows having E/D on either pin 1 or pin 2.

For Optimum Jitter Performance, Pletronics recommends:

- A ground plane under the device with any other signals below the ground plane
- Minimize other RF signals near device
- No large transient signals (both current and voltage) should be routed under the device
- Do not layout near a large magnetic field such as a high frequency switching power supply
- Do not place near piezoelectric buzzers or mechanical fans



Mar 2004



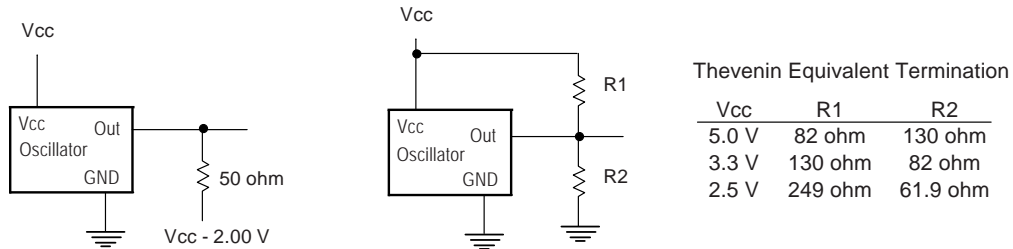
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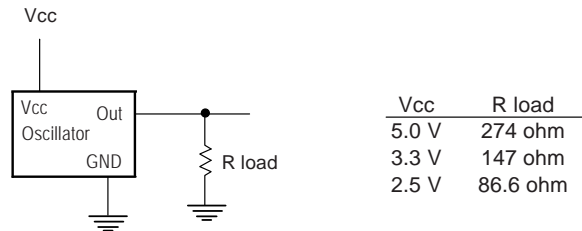
## PECL and LVDS Layout Guidelines Continued

### PECL Terminations:

Suggested Terminations for 50 ohm impedance matched termination



Simple termination for NON impedance matched termination



### LVDS Terminations:



### Mixed System Power Supply:

- PECL** To use multiple supply voltages requires level translation. Direct circuit connection is not valid.
- ECL** Mixed supply voltages are allowed. No translation is necessary. (ECL is returned to the most positive supply and this is common to all circuits)
- LVDS** Mixed supply voltages are allowed. LVDS signal levels are power supply independent. 3.3 V LVDS oscillators properly interface 2.5 V Logic Arrays for example.

Mar 2004