

LV96/LV98 Series 3.3 V LVDS Clock Oscillators

February 2016



- Pletronics LV96/LV98 Series is a quartz crystal controlled precision square wave generator with an LVDS output.
- Solder pad compatible legacy LVDS oscillator solutions.
- FR4 base using the LV93 or LV99 5x7 mm ceramic packaged SMD device.
- Tape and Reel packaging is available.
- 10.9 to 670 MHz
- Enable/Disable Function:
 - **LV98** on pad 2
 - **LV96** on pad 1
- Low Jitter

***This series, LV96 and LV98, is not recommended for new designs.
* For new designs, pin-out on pad 1 is the only available option for LV99 series part.***

**Pletronics Inc. certifies this device is in accordance with the
RoHS 6/6 (2011/65/EC) and WEEE (2002/96/EC) directives.**

Pletronics Inc. guarantees the device does not contain the following:
Cadmium, Hexavalent Chromium, Lead, Mercury, PBB's, PBDE's
Weight of the Device: 0.40 grams
Moisture Sensitivity Level: 1 As defined in J-STD-020C
Second Level Interconnect code: e4

Absolute Maximum Ratings:

Parameter	Unit
V _{CC} Supply Voltage	-0.5V to +6.5V
V _i Input Voltage	-0.5V to V _{CC} + 0.5V
V _o Output Voltage	-0.5V to V _{CC} + 0.5V

Thermal Characteristics

The maximum die or junction temperature is 155°C
The thermal resistance junction to board is 40 to 80°C/Watt depending on the solder pads, ground plane and construction of the PCB.

Part Number:

LV9x	45	D	E	V	-125.0M	-XX	
							Packaging code or blank T250 = 250 per Tape and Reel T500 = 500 per Tape and Reel T1K = 1000 per Tape and Reel
							Frequency in MHZ
							Supply Voltage V_{CC} V = 3.3V ± 10%
							Temperature Range blank = -10 to +70°C C = -20 to +70°C E = -40 to +85°C
							Series Model
							Frequency Stability 45 = ± 50 ppm 44 = ± 25 ppm 20 = ± 20 ppm
							Series Model (x is 6 or 8)

Part Marking:

PLE LV9x
FF.FFF M
• YMDXX

Marking Legend:

PLE = Pletronics X = 6 or 8
 FF.FFF M = Frequency in MHZ
 YMD = Date of Manufacture (year-month-day)
 All other marking is internal factory codes

Codes for Date Code YMD

Code	4	5	6	7	8	Code	A	B	C	D	E	F	G	H	J	K	L	M
Year	2014	2015	2016	2017	2018	Month	JAN	FEB	MAR	APR	MAY	JUN	JUL	AUG	SEP	OCT	NOV	DEC

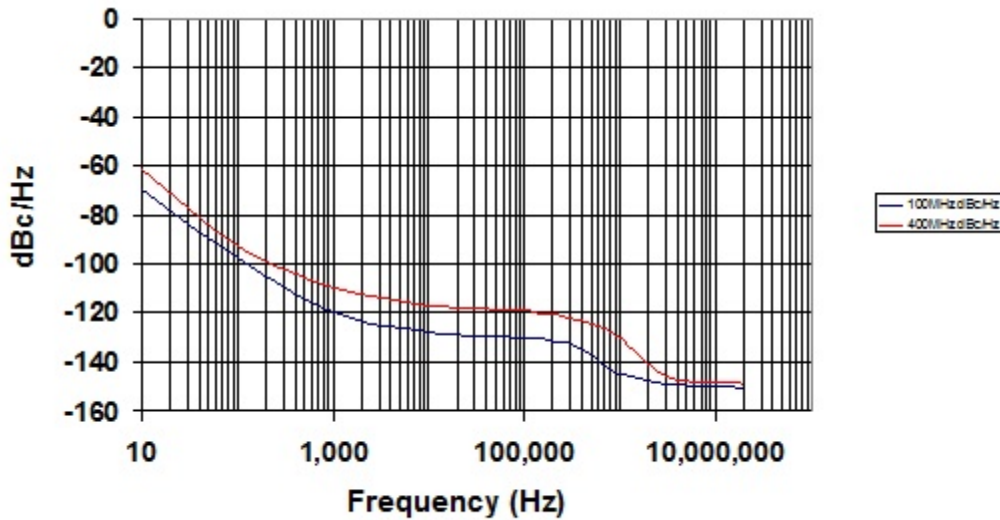
Code	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	G
Day	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Code	H	J	K	L	M	N	P	R	T	U	V	W	X	Y	Z	
Day	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	

Electrical Specification for 3.30V \pm 10% over the specified temperature range and the frequency range of 10.9 MHz to 670 MHz

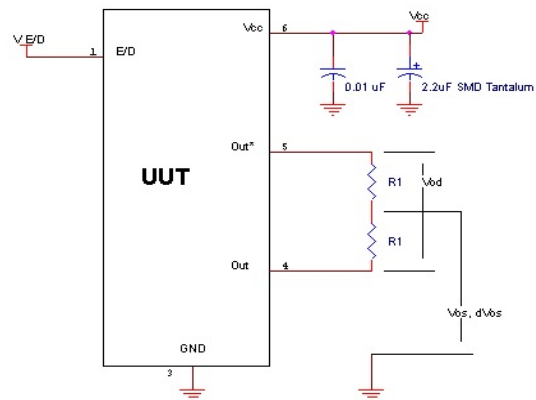
Item	Min	Max	Unit	Condition	
Frequency Accuracy	"45"	-50	+50	ppm	For all supply voltages, load changes, aging for 1 year, shock, vibration and temperatures
	"44"	-25	+25		
	"20"	-20	+20		
Output Waveform	LVDS				
Output High Level	--	1.60	Volts	See load circuit R1 = 50 ohms	
Output Low Level	0.90	--	Volts		
Differential Output (V_{OD})	250	450	mVolts		
Output Offset Voltage (V_{OS})	1.125	1.375	Volts		
Differential Output Error (dV_{OS})	--	50	mVolts		
Output Symmetry	47	53	%	Referenced to 50% of amplitude or crossing point	
Output T_{RISE} and T_{FALL}	150	230	pS	Vth is 20% and 80% of waveform	
Jitter	-	0.6	pS RMS	Measured from 12KHz to 20MHz from Fnominal	
	-	2.8		Measured from 10Hz to 20MHz from Fnominal	
Output Short Circuit Current	-	-20	mA	Vout = 0.0V	
Vcc Supply Current	-	80	mA		
Enable/Disable Internal Pull-up	50	-	Kohm	To Vcc (equivalent resistance)	
V disable	-	0.8	Volts	Referenced to Ground	
V enable	2.0	-	Volts	Referenced to Ground	
Output leakage	$V_{OUT} = V_{CC}$	-20	+20	uA	Pad 1 low, device disabled
	$V_{OUT} = 0V$	-20	+20		
Enable	-	10	nS	Time for output to reach a logic state	
Disable time	-	10	nS	Time for output to reach a high Z state	
Start up time	-	5	mS	Measured from the time Vcc = 3.0V	
Operating Temperature Range	-10	+70	°C	Standard Temperature Range	
	-20	+70	°C	Extended Temperature Range "C" Option	
	-40	+85	°C	Extended Temperature Range "E" Option	
Storage Temperature Range	-55	+125	°C		

Specifications with E/D open circuit or connected to V_{CC}

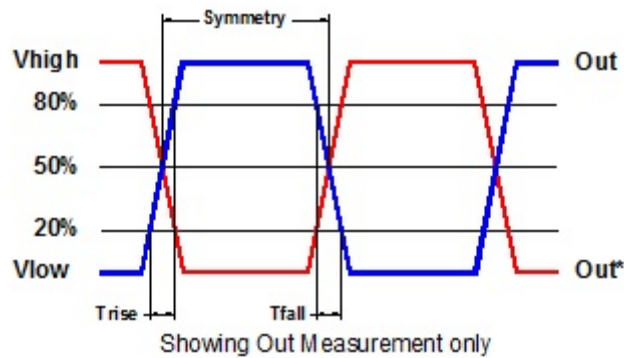
Typical Phase-Noise Response



Load Circuit



Test Waveform



Reliability: Environmental Compliance

Parameter	Condition
Mechanical Shock	MIL-STD-883 Method 2002, Condition B
Vibration	MIL-STD-883 Method 2007, Condition A
Solderability	MIL-STD-883 Method 2003
Thermal Shock	MIL-STD-883 Method 1011, Condition A

ESD Rating

Model	Minimum Voltage	Conditions
Human Body Model	1500	MIL-STD-883 Method 3115
Charged Device Model	1000	JESD 22-C101

Package Labeling

Label is 1" x 2.6" (25.4mm x 66.7mm)






Font is Courier New

Bar code is 39-Full ASCII

(The part number will show as LV96xx or LV98xx)

Label is 1" x 2.6" (25.4mm x 66.7mm)

Font is Arial

P/N:		
	LV9920DV-312 . 50M	
Customer P/N:		
	12345678	
Qty:		D/C 
	1000	7AA-BT

RoHS Compliant
2nd Lvl Interconnect
Category=e4
Max Safe Temp=245C for 10s 2X Max

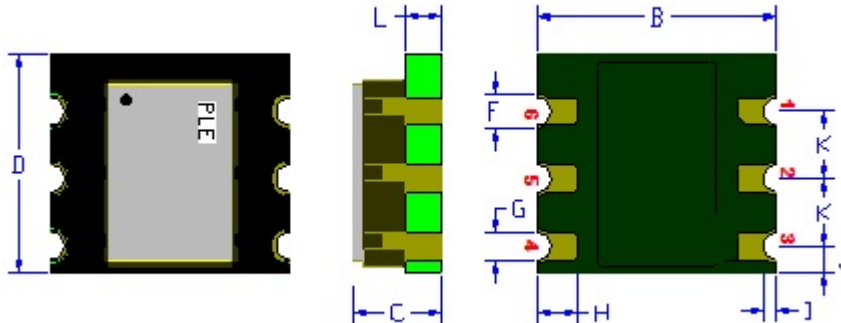
Layout and application information

For Optimum Jitter Performance, Pletronics recommends:

- a ground plane under the device
- no large transient signals (both current and voltage) should be routed under the device
- do not layout near a large magnetic field such as a high frequency switching power supply
- do not place near piezoelectric buzzers or mechanical fans.

As much ground plane and thermal paths that can be realized under and to the side of the part is desired.

Mechanical:



Label:
laser marked lettering

FR4 PCB Base:
Solder masked

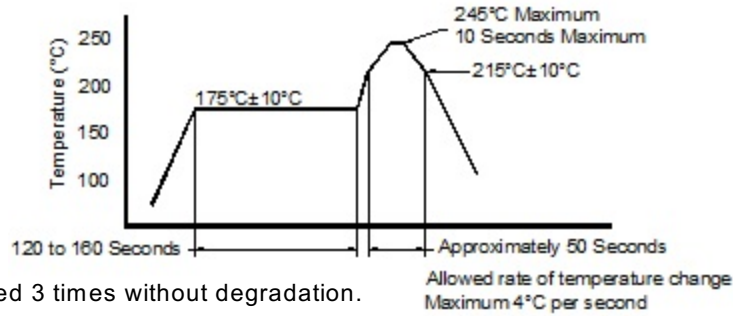
All via holes tented on bottom
Copper Clad 670 μ inch (17 μ m)
Nickel plated 118 μ inch (3 μ m)
Gold plated 0.8 μ inch (0.02 μ m)
Typical thicknesses

Pin 3 Ground plane is typical
Not to scale

	Inches	mm
B	0.356 \pm 0.005	9.04 \pm 0.13
C	0.126 \pm 0.005	3.21 \pm 0.13
D	0.324 \pm 0.005	8.23 \pm 0.13
F ¹	0.050	1.27
G ¹	0.040	1.02
H ¹	0.059	1.50
I ¹	0.020	0.51
J ¹	0.040	1.02
K ¹	0.100	2.54
L ¹	0.062	1.57

LV98 Pad	LV96 Pad	Function	Note
2	1	Output Enable/Disable	When this pad is not connected the oscillator shall operate. This is not a recommended condition!!!!!! When this pad is <0.80 volts, the output will be inhibited (High impedance state) Recommend connecting this pad to V_{CC} if the oscillator is to be always on.
1	2	No function	Recommend connecting this pad to ground. The is internal connection.
3		Ground (GND)	
4		Output	The outputs must be terminated, 100 ohms between the outputs is the ideal termination. Capacitor coupled terminations can be used.
5		Output*	
6		Supply Voltage (V_{CC})	Recommend connecting appropriate power supply bypass capacitors as close as possible.

Reflow Cycle (typical for lead free processing)



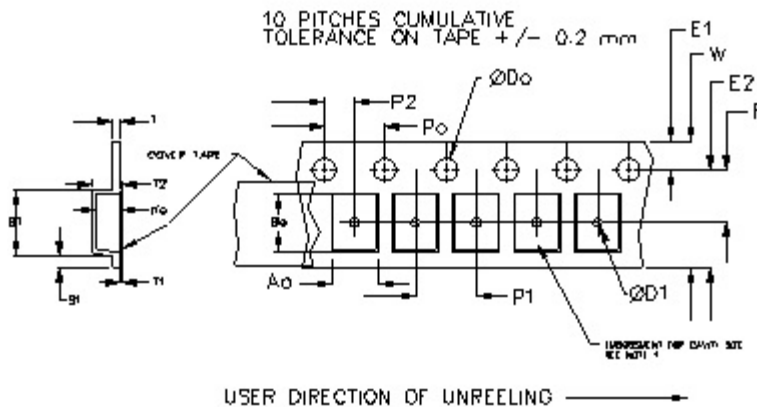
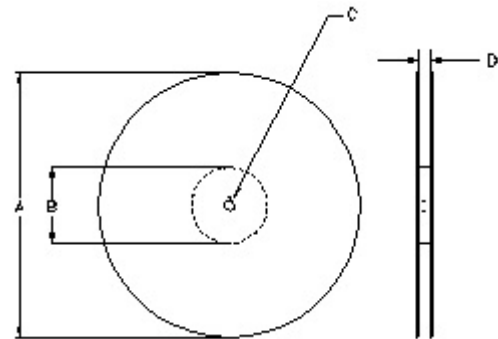
The part may be reflowed 3 times without degradation.

Tape and Reel: available for quantities of 250 to 1000 per reel

Constant Dimensions Table 1								
Tape Size	D0	D1 Min	E1	P0	P2	S1 Min	T Max	T1 Max
8mm	+0.1 -0.0	1.0	1.75	4.0	2.0 ±0.05	0.6	0.6	0.1
12mm		1.5			2.0 ±0.1			
16mm		1.5						
24mm		1.5						

Variable Dimensions Table 2							
Tape Size	B1 Max	E2 Min	F	P1	T2 Max	W Max	Ao, Bo & Ko
24 mm	12.1	14.25	7.5 ±0.1	16.0 ±0.1	8.0	16.3	Note 1

Note 1: Embossed cavity to conform to EIA-481-B Dimensions in mm Not to scale



REEL DIMENSIONS					
A	inches	7.0	10.0	13.0	Tape Width
	mm	177.8	254.0	330.2	
B	inches	2.50	4.00	3.75	Tape Width
	mm	63.5	101.6	95.3	
C	mm	13.0 +0.5 / -0.2			Tape Width
D	mm	---	---	24.4 +2.0 -0.0	

Reel dimensions may vary from the above

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PLETRONICS INC. DOCUMENT CONTROL

This is the document control page. **This is not printed or part of the PDF that can be downloaded on the web site.** This is to keep the history of the datasheet document and all revisions.

Part Number Family: LVDS 99 Series
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PDF File Name: lv96 lv98.pdf
Written By: R Gubser
Approved By:

Revision History:

January 2008 Initial Release

April 26, 2010 Added the "C" temperature range, Added 3 reflows Rag

February 3, 2016 Updated company logo, RoHS information and date code range.